PCT WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : H04L 12/56

A2

(11) International Publication Number: **WO 99/21326**

(43) International Publication Date: 29 April 1999 (29.04.99)

(21) International Application Number: PCT/FI98/00816

(22) International Filing Date: 20 October 1998 (20.10.98)

(30) Priority Data:
974020 21 October 1997 (21.10.97) FI

(71) Applicant *(for all designated States except US)*: NOKIA TELECOMMUNICATIONS OY [FI/FI]; Keilalahdentie 4, FIN–02150 Espoo (FI).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: KORHONEN, Jari [FI/FI]; Kauppiaantie 2, FIN–10300 Karjaa (FI). SUVANEN, Jyri [FI/FI]; Väinö Auerin katu 1 G 24, FIN–00560 Helsinki (FI). LEHTIMÄKI, Matti [FI/FI]; Kyyhkysmäki 16 A 4, FIN–02600 Espoo (FI).

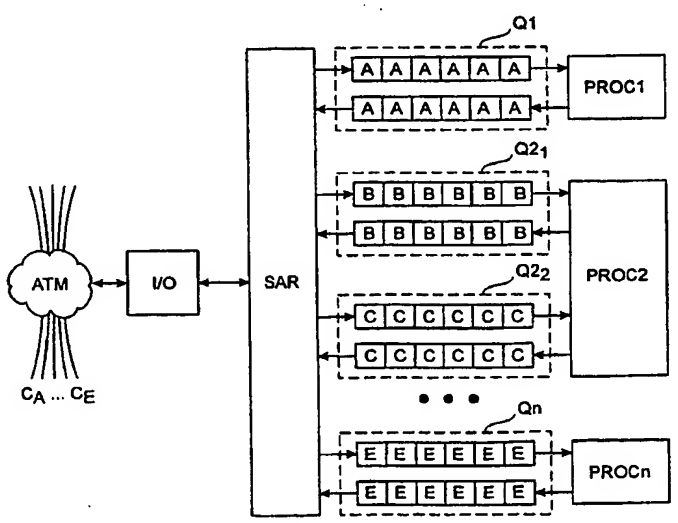
(74) Agent: KOLSTER OY AB; Iso Roobertinkatu 23, P.O. Box 148, FIN–00121 Helsinki (FI).

(81) Designated States: AL, AM, AT, AT (Utility model), AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, CZ (Utility model), DE, DE (Utility model), DK, DK (Utility model), EE, EE (Utility model), ES, FI, FI (Utility model), GB, GD, GE, GH, GM, HR, HU, ID, IL, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SK (Utility model), SL, TJ, TM, TR, TT, UA, UG, US, UZ, VN, YU, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Published

In English translation (filed in Finnish).
Without international search report and to be republished upon receipt of that report.

(54) Title: RESOURCE OPTIMIZATION IN A MULTIPROCESSOR SYSTEM FOR A PACKET NETWORK



(57) Abstract

A method, an arrangement and an SAR circuit for serving several packet switched telecommunication connections (C_A to C_E) by several processors (PROC1 to PROCn). One processor is selected from among several processors (PROC1 to PROCn) for each telecommunication connection (C_A to C_E) to be served. On each telecommunication connection (C_A to C_E) information is transmitted in packets from which are formed elements (A to E) of at least one queue (Q1 to Qn). A separate queue (Q1 to Qn) is formed for each telecommunication connection (C_A to C_E) to be served. The SAR circuit conveys only queue elements (A to E) formed from the packets of the respective telecommunication connection (C_A to C_E) via each queue to a corresponding processor (PROC1 to PROCn).

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AL	Albania	**ES**	Spain	**LS**	Lesotho	**SI**	Slovenia
AM	Armenia	**FI**	Finland	**LT**	Lithuania	**SK**	Slovakia
AT	Austria	**FR**	France	**LU**	Luxembourg	**SN**	Senegal
AU	Australia	**GA**	Gabon	**LV**	Latvia	**SZ**	Swaziland
AZ	Azerbaijan	**GB**	United Kingdom	**MC**	Monaco	**TD**	Chad
BA	Bosnia and Herzegovina	**GE**	Georgia	**MD**	Republic of Moldova	**TG**	Togo
BB	Barbados	**GH**	Ghana	**MG**	Madagascar	**TJ**	Tajikistan
BE	Belgium	**GN**	Guinea	**MK**	The former Yugoslav Republic of Macedonia	**TM**	Turkmenistan
BF	Burkina Faso	**GR**	Greece			**TR**	Turkey
BG	Bulgaria	**HU**	Hungary	**ML**	Mali	**TT**	Trinidad and Tobago
BJ	Benin	**IE**	Ireland	**MN**	Mongolia	**UA**	Ukraine
BR	Brazil	**IL**	Israel	**MR**	Mauritania	**UG**	Uganda
BY	Belarus	**IS**	Iceland	**MW**	Malawi	**US**	United States of America
CA	Canada	**IT**	Italy	**MX**	Mexico	**UZ**	Uzbekistan
CF	Central African Republic	**JP**	Japan	**NE**	Niger	**VN**	Viet Nam
CG	Congo	**KE**	Kenya	**NL**	Netherlands	**YU**	Yugoslavia
CH	Switzerland	**KG**	Kyrgyzstan	**NO**	Norway	**ZW**	Zimbabwe
CI	Côte d'Ivoire	**KP**	Democratic People's Republic of Korea	**NZ**	New Zealand		
CM	Cameroon			**PL**	Poland		
CN	China	**KR**	Republic of Korea	**PT**	Portugal		
CU	Cuba	**KZ**	Kazakstan	**RO**	Romania		
CZ	Czech Republic	**LC**	Saint Lucia	**RU**	Russian Federation		
DE	Germany	**LI**	Liechtenstein	**SD**	Sudan		
DK	Denmark	**LK**	Sri Lanka	**SE**	Sweden		
EE	Estonia	**LR**	Liberia	**SG**	Singapore		

RESOURCE OPTIMIZATION IN A MULTIPROCESSOR SYSTEM FOR A PACKET NETWORK

BACKGROUND OF THE INVENTION

The invention relates to serving packet switched connections, preferably ATM connections, in a multiprocessor system, and particularly to optimizing resource allocation in such a system. The invention further relates to an SAR circuit employed in such a system.

With reference to Figure 1, in a packet switched network information is transmitted in packets comprising at least a header part and a payload part. In an ATM network, for example, the length of the packets is 53 bytes. A five-byte header indicates with which connection the packet in question is associated. For the sake of simplicity, Figure 1 shows five connections C_A to C_E. A terminal using ATM connections is typically a workstation, a personal computer or the like wherein one efficient processor PROC1 processes the ATM connections. The ATM terminal equipment comprises an SAR circuit (Segmentation And Re-assembly) SAR which receives ATM packets and writes them to a queue Q1 located in a memory, from which queue the processor retrieves them on a first in, first out principle (FIFO).

If more than one processor are needed in the terminal equipment, the allocation of resources between the different processors presents a problem. In accordance with a potential solution, one common SAR circuit shared by all processors serves all processors sharing a common queue. In this solution the elements of the queue are formed in an unarranged manner from packets which belong to all C_A to C_E. The processors spend much time searching the queue Q1 only for elements which belong to them. Furthermore, to write to a shared queue would be difficult for the processors. If, on the other hand, there are as many queues as there are processors but the SAR circuit is still a shared one, the processors still waste their time searching the unarranged queues only for elements which belong to them. If a specific SAR circuit is reserved for each processor, the queues could be arranged in such a manner that only elements which belong to the respective processor are written to the queue of each processor. The problem in this solution is, however, that it requires a great number of SAR circuits, and it is still unclear how the system should be configured in case some processors serve more than one connection at a time.

This is not extremely harmful in terminal equipment with a light processing load associated with a single connection, since the processors can perform the required arranging (for example by simply selecting only packets which belong to the connection to be served and discarding others). In network elements performing complex signal processing, such as speech encoding devices, echo cancellers, compression or decompression devices, etc. the situation is different. One processor (typically a digital signal processor DSP) can usually serve a few connections at the most and often only one connection at a time. The processors spend much time arranging the queues according to which connection they serve at a given time.

BRIEF DESCRIPTION OF THE INVENTION

An object of the invention is thus to provide a method and equipment implementing the method so as to solve the above problems. More specifically, the object of the invention is to enable resources to be more efficiently utilized in a multiprocessor system which serves several connections. The objects of the invention can be achieved by a method, an arrangement and an SAR circuit characterized by what is said in the independent claims. The preferred embodiments of the invention are disclosed in the dependent claims.

The invention is based on the idea of forming a separate queue for each telecommunication connection to be served in a memory space of an SAR circuit, and conveying to each queue substantially only queue elements formed from packets which belong to the respective telecommunication connection. In this connection, "substantially only" means that only queue elements formed from packets of a corresponding telecommunication connection (but not of other connections) are transmitted via each queue. Furthermore, processor configuration instructions and status information may be transmitted via the queue. In the present invention, this configuring means that the processor is informed at which memory address the queues associated with the connections and served by it can be found. Most preferably, all queues and processors share a common SAR circuit. Each queue can in practice be implemented as a ring buffer pair or a linked list. The SAR circuit places in each queue only packets which belong to the connection corresponding to it. If a processor serves several connections, the processor also processes several queues.

An advantage of the method and the system of the invention is that the processors do not have to spend much time arranging the queues, and the equipment becomes readily scalable for large numbers of connections and processors. Avoiding redundant processing also reduces power consumption. The memory capacity required by the queues is reduced since no need exists to store in any queue packets which will not be processed. In accordance with a preferred embodiment, a shared SAR circuit is fitted for several processors, which reduces the number of components and the price of the system. The invention thus enables several processors to be connected behind a shared SAR circuit.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention is now described in closer detail in connection with the preferred embodiments with reference to the accompanying drawings, in which

Figure 1 shows how several connections are served by one processor in accordance with prior art, and

Figure 2 shows how several connections are served by several processors in accordance with the invention.

DETAILED DESCRIPTION OF THE INVENTION

Let us first take a simple case in which packets A to E which belong to connections C_A to C_E can be processed as such. An example of such a situation is a speech frame of the GSM system, whose length is about 85% of the length of the payload of an ATM cell.

With reference to Figure 2, a shared SAR circuit arranges packets which belong to all connections C_A to C_E into queues Q1 to Q2 on the basis of their header in such a manner that a separate queue is formed in the memory space of the SAR circuit for each connection C_A to C_E. The SAR circuit places in each queue Q1 to Qn only packets which belong to a corresponding connection C_A to C_E. The queues Q1 to Qn can be provided in a shared physical memory. A problem is then presented, however, by collisions caused by several processors simultaneously writing in the same memory. Even if the queue of each processor was located in a separate storage area, the processor would be compelled to use the same data and/or address bus simultaneously. It is thus more preferable to implement a separate physical queue for each processor. In accordance with a preferred embodiment, in order to save mem-

ory only the payload parts of the packets are stored in the queues Q1 to Qn and the packet header parts are reformed when the packet is transmitted to the network after processing. Since the length of the packet is a fixed one in this example, the queues Q1 to Qn can be simple ring buffer pairs in which the writing element (the SAR circuit or the processor) maintains the write address of a next location, rewrites the packet to this address and increments the write address. The reading element (the processor or the SAR circuit, correspondingly) reads the packet from the read address of the location to be read next and increments this address. When the write or the read address is incremented beyond the maximum address of the ring buffer, it is returned to the minimum address.

A situation in which the same processor serves several connections (in this case C_B and C_C) is shown in connection with a second processor of Figure 2. The processor PROC2 reads from and writes to two queues $Q2_1$ and $Q2_2$. A separate queue is provided for each connection C_A to C_E, however.

Let us next discuss a more complex case in which the packets A to E which belong to the connections C_A to C_E do not as such constitute appropriate packets to be processed. Such a situation is, for example, a half-speed speech frame of the GSM system, two of which fit in one ATM cell. On such a connection, the SAR circuit can be configured to divide the payload of one ATM cell into two packets to a corresponding queue Q1 to Qn. Similarly, if the length of the packet to be processed is a fixed multiple of the payload of the ATM cell, the SAR circuit can be configured to form each packet of the queue from the payload part of several ATM cells. In all the cases described above the queues Q1 to Qn can be implemented as ring buffers, for example.

However, if variable length packets produced by many video codecs, for example, are transmitted via the ATM network, a simple ring buffer is not sufficient but the queues can be formed as linked lists, for example, in which each element refers to the beginning of a next element.

It is obvious to those skilled in the art that with progress in technology the basic ideas of the invention can be implemented in various ways. The invention and its embodiments are thus not restricted to the examples described above, but they can vary within the scope of the claims.

CLAIMS

1. A method of serving several packet switched telecommunication connections (C_A to C_E) by several processors (PROC1 to PROCn), in which method

one of several processors (PROC1 to PROCn) is selected to serve each connection (C_A to C_E) to be served,

on each telecommunication connection (C_A to C_E) information is transmitted in packets from which are formed elements (A to E) of at least one queue (Q1 to Qn) and which elements are conveyed via said queue to said selected processor (PROC1 to PROCn),

characterized in that

a separate queue (Q1 to Qn) is formed for each telecommunication connection (C_A to C_E) to be served, and to each queue substantially only queue elements (A to E) formed from packets of the respective telecommunication connection (C_A to C_E) are conveyed.

2. A method as claimed in claim 1, **characterized** in that said telecommunication connection packets comprise a header part and a payload part and the elements (A to E) of said queues (Q1 to Qn) are formed from a fixed number of payload parts of the packets.

3. A method as claimed in claim 2, **characterized** in that the queues (Q1 to Qn) are formed as pairs of ring buffers, one ring buffer comprising elements (A to E) applied to the processor and the other ring buffer comprising elements (A to E) supplied from the processor.

4. A method as claimed in claim 1, **characterized** in that said telecommunication connection packets comprise a header part and a payload part, and the elements (A to E) of said queues (Q1 to Qn) are formed from a variable number of payload parts of the packets.

5. A method as claimed in claim 4, **characterized** in that the queues (Q1 to Qn) are formed as pairs of linked lists, one list comprising packets (A to E) or their payload parts applied to the processor, and the other list comprising packets (A to E) or their payload parts supplied from the processor.

6. An arrangement for serving several telecommunication connections (C_A to C_E) by several processors (PROC1 to PROCn), which arrangement comprises

connection means (I/O) for connecting to a telecommunications network (ATM) in which information is transmitted in packets,

means for selecting one processor from among several processors (PROC1 to PROCn) to serve each said telecommunication connection (C_A to C_E), and at least one queue (Q1 to Qn),

segmentation means (SAR) operationally connected to said connection means (I/O) for forming queue elements (A to E) from said packets and conveying the elements (A to E) via said queue (Q1 to Qn) to the processor (PROC1 to PROC2) selected to serve the respective communication connection (C_A to C_E) and vice versa,

characterized in that the arrangement is arranged to form a separate queue (Q1 to Qn) for each telecommunication connection (C_A to C_E) to be served and to convey to each queue (Q1 to Qn) substantially only queue elements (A to E) formed from the packets of the respective telecommunication connection (C_A to C_E).

7. An arrangement as claimed in claim 6, **characterized** in that said packets are ATM frames and said segmentation means comprise a common SAR circuit (SAR) shared by all queues and processors.

8. A segmentation circuit and a re-assembly circuit, i.e. an SAR circuit, of a packet switched telecommunications network, particularly of an ATM network, which circuit is arranged to read packets which belong to the different connections (C_A to C_E) of said telecommunications network, and to form from the packets elements (A to E) of at least one queue (Q1), **characterized** in that the SAR circuit is arranged to connect to several queues (Q1 to Qn) of which one is provided for each telecommunication connection (C_A to C_E) to be served, and to place in each queue (Q1 to Qn) substantially only queue elements (A to E) formed from the packets of the respective telecommunication connection (C_A to C_E).

Fig. 1
(PRIOR ART)

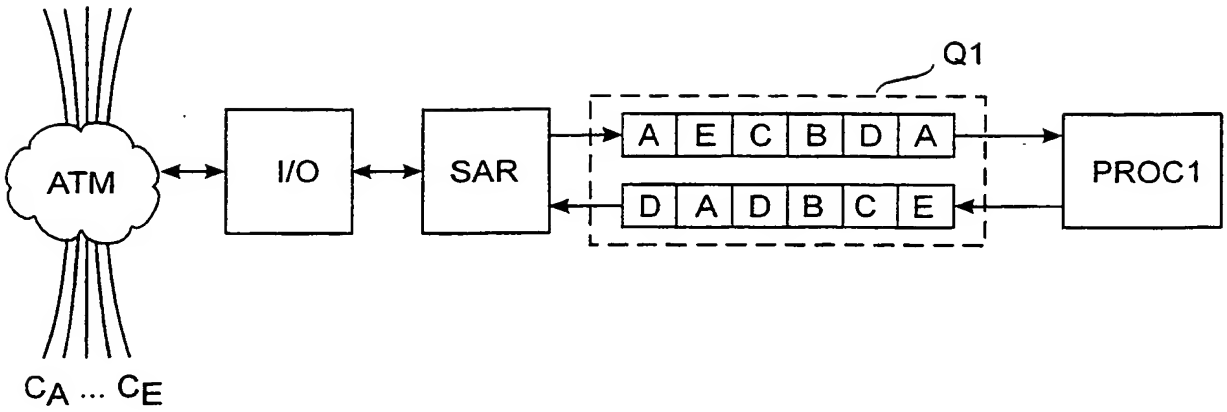
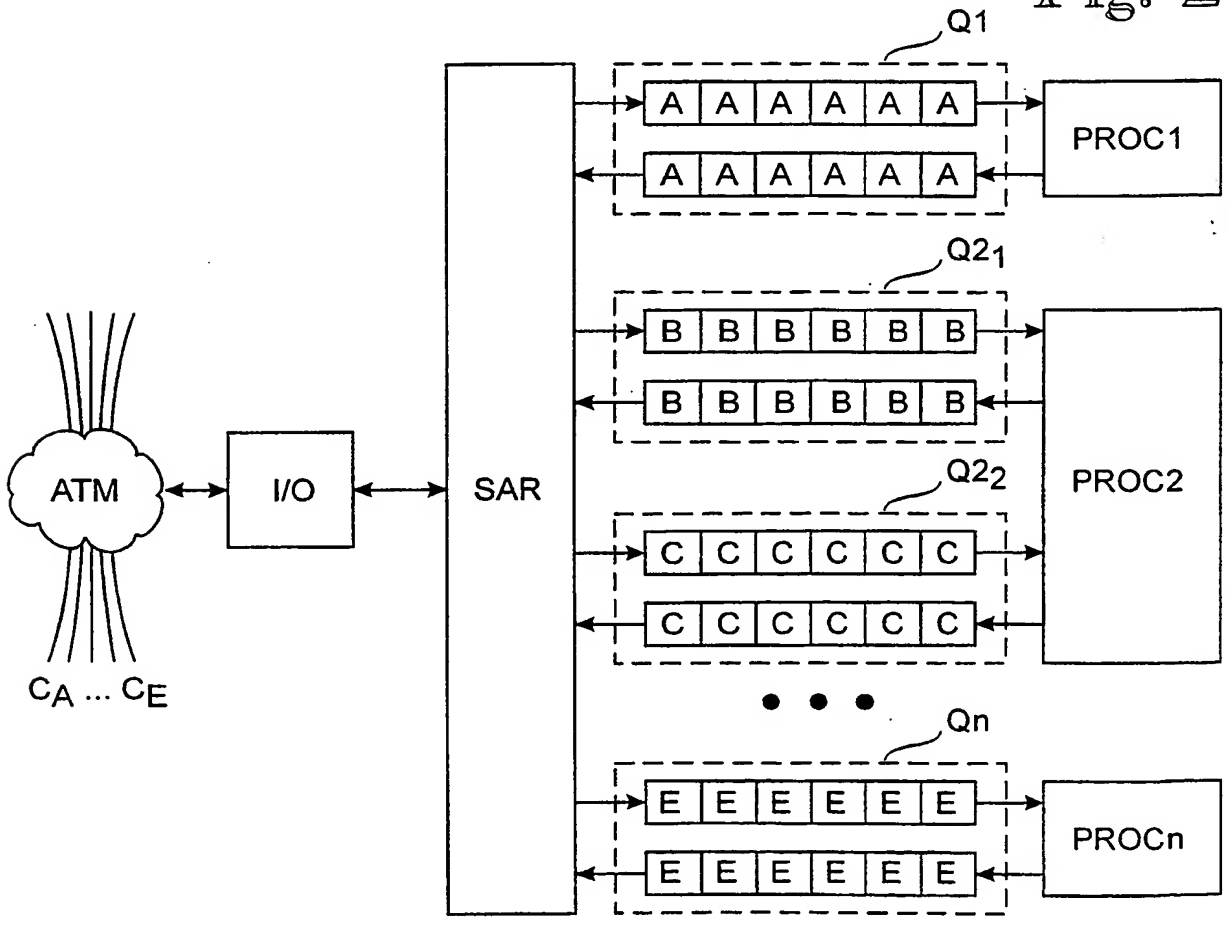


Fig. 2



PCT WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 :
H04L 12/56, H04Q 11/04

A3

(11) International Publication Number: **WO 99/21326**

(43) International Publication Date: 29 April 1999 (29.04.99)

(21) International Application Number: PCT/FI98/00816

(22) International Filing Date: 20 October 1998 (20.10.98)

(30) Priority Data:
974020 21 October 1997 (21.10.97) FI

(71) Applicant *(for all designated States except US)*: NOKIA TELECOMMUNICATIONS OY [FI/FI]; Keilalahdentie 4, FIN–02150 Espoo (FI).

(72) Inventors; and
(75) Inventors/Applicants *(for US only)*: KORHONEN, Jari [FI/FI]; Kauppiaantie 2, FIN–10300 Karjaa (FI). SUVANEN, Jyri [FI/FI]; Väinö Auerin katu 1 G 24, FIN–00560 Helsinki (FI). LEHTIMÄKI, Matti [FI/FI]; Kyyhkysmäki 16 A 4, FIN–02600 Espoo (FI).

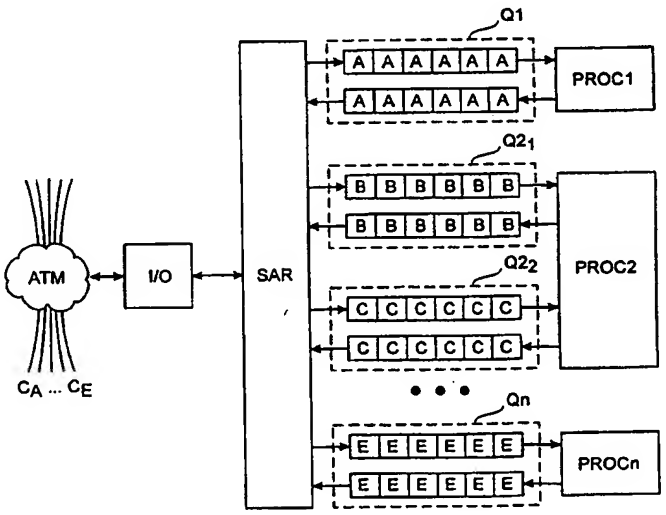
(74) Agent: KOLSTER OY AB; Iso Roobertinkatu 23, P.O. Box 148, FIN–00121 Helsinki (FI).

(81) Designated States: AL, AM, AT, AT (Utility model), AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, CZ (Utility model), DE, DE (Utility model), DK, DK (Utility model), EE, EE (Utility model), ES, FI, FI (Utility model), GB, GD, GE, GH, GM, HR, HU, ID, IL, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SK (Utility model), SL, TJ, TM, TR, TT, UA, UG, US, UZ, VN, YU, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Published
With international search report.
In English translation (filed in Finnish).

(88) Date of publication of the international search report:
29 July 1999 (29.07.99)

(54) Title: RESOURCE OPTIMIZATION IN A MULTIPROCESSOR SYSTEM FOR A PACKET NETWORK



(57) Abstract

A method, an arrangement and an SAR circuit for serving several packet switched telecommunication connections (C_A to C_E) by several processors (PROC1 to PROCn). One processor is selected from among several processors (PROC1 to PROCn) for each telecommunication connection (C_A to C_E) to be served. On each telecommunication connection (C_A to C_E) information is transmitted in packets from which are formed elements (A to E) of at least one queue (Q1 to Qn). A separate queue (Q1 to Qn) is formed for each telecommunication connection (C_A to C_E) to be served. The SAR circuit conveys only queue elements (A to E) formed from the packets of the respective telecommunication connection (C_A to C_E) via each queue to a corresponding processor (PROC1 to PROCn).

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AL	Albania	**ES**	Spain	**LS**	Lesotho	**SI**	Slovenia
AM	Armenia	**FI**	Finland	**LT**	Lithuania	**SK**	Slovakia
AT	Austria	**FR**	France	**LU**	Luxembourg	**SN**	Senegal
AU	Australia	**GA**	Gabon	**LV**	Latvia	**SZ**	Swaziland
AZ	Azerbaijan	**GB**	United Kingdom	**MC**	Monaco	**TD**	Chad
BA	Bosnia and Herzegovina	**GE**	Georgia	**MD**	Republic of Moldova	**TG**	Togo
BB	Barbados	**GH**	Ghana	**MG**	Madagascar	**TJ**	Tajikistan
BE	Belgium	**GN**	Guinea	**MK**	The former Yugoslav Republic of Macedonia	**TM**	Turkmenistan
BF	Burkina Faso	**GR**	Greece			**TR**	Turkey
BG	Bulgaria	**HU**	Hungary	**ML**	Mali	**TT**	Trinidad and Tobago
BJ	Benin	**IE**	Ireland	**MN**	Mongolia	**UA**	Ukraine
BR	Brazil	**IL**	Israel	**MR**	Mauritania	**UG**	Uganda
BY	Belarus	**IS**	Iceland	**MW**	Malawi	**US**	United States of America
CA	Canada	**IT**	Italy	**MX**	Mexico	**UZ**	Uzbekistan
CF	Central African Republic	**JP**	Japan	**NE**	Niger	**VN**	Viet Nam
CG	Congo	**KE**	Kenya	**NL**	Netherlands	**YU**	Yugoslavia
CH	Switzerland	**KG**	Kyrgyzstan	**NO**	Norway	**ZW**	Zimbabwe
CI	Côte d'Ivoire	**KP**	Democratic People's Republic of Korea	**NZ**	New Zealand		
CM	Cameroon			**PL**	Poland		
CN	China	**KR**	Republic of Korea	**PT**	Portugal		
CU	Cuba	**KZ**	Kazakstan	**RO**	Romania		
CZ	Czech Republic	**LC**	Saint Lucia	**RU**	Russian Federation		
DE	Germany	**LI**	Liechtenstein	**SD**	Sudan		
DK	Denmark	**LK**	Sri Lanka	**SE**	Sweden		
EE	Estonia	**LR**	Liberia	**SG**	Singapore		

INTERNATIONAL SEARCH REPORT

International application No.
PCT/FI 98/00816

A. CLASSIFICATION OF SUBJECT MATTER

IPC6: H04L 12/56, H04Q 11/04
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC6: H04L, H04Q

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

SE,DK,FI,NO classes as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPOC, WPIL, JAPIO, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 9725831 A1 (CISCO SYSTEMS, INC.), 17 July 1997 (17.07.97), page 8, line 1 - page 9, line 21, figure 3, claims 1-4, abstract --	1,6-8
X	WO 9725803 A1 (CISCO SYSTEMS, INC.), 17 July 1997 (17.07.97), page 8, line 3 - page 10, line 11, figures 3-5, claims 7-13, abstract --	1,6-8
A	US 5414702 A (NORIMASA KUDOH), 9 May 1995 (09.05.95), column 2, line 31 - line 68; column 3, line 31 - column 5, line 53, figures 1-3, claims 1-3, abstract --	1-8

[X] Further documents are listed in the continuation of Box C. [X] See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" erlier document but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance: the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance: the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
19 May 1999	19 -05- 1999
Name and mailing address of the ISA/ Swedish Patent Office Box 5055, S-102 42 STOCKHOLM Facsimile No. +46 8 666 02 86	Authorized officer Erik Johannesson Telephone No. +46 8 782 25 00

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/FI 98/00816

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5428609 A (KAI Y. ENG ET AL), 27 June 1995 (27.06.95), see the whole document ---	1-8
A	EP 0763915 A2 (KABUSHIKI KAISHA TOSHIBA), 19 March 1997 (19.03.97), page 5, line 57 - page 7, line 6; page 8, line 16 - page 10, line 20, figure 5, claims 1-10, abstract --- --------	1-8

INTERNATIONAL SEARCH REPORT

Information on patent family members

03/05/99

International application No.
PCT/FI 98/00816

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO 9725831 A1	17/07/97	AU 1530797 A	01/08/97
		US 5765032 A	09/06/98
WO 9725803 A1	17/07/97	AU 1530897 A	01/08/97
		US 5838994 A	17/11/98
US 5414702 A	09/05/95	CA 2108863 A	21/04/94
		JP 6132974 A	13/05/94
US 5428609 A	27/06/95	NONE	
EP 0763915 A2	19/03/97	JP 9149051 A	06/06/97